A 5-GHz Monolithic Silicon Bipolar Down-converter with a 3.2-dB Noise Figure

Alessandro Italia [1], Egidio Ragonese [1], Giovanni Girlando [2], and Giuseppe Palmisano [1]

[1] Università di Catania, Facoltà di Ingegneria, DIEES V.le A. Doria 6, 95125, Catania, Italia
[2] STMicroelectronics, Str.le Primosole 50, 95121, Catania, Italia
E-mail: aitalia@diees.unict.it, eragone@diees.unict.it, giovanni.girlando@st.com, gpalmisano@diees.unict.it

Abstract **— A monolithic 5-GHz down-converter consisting of a low noise amplifier (LNA) and a double-balanced mixer was designed using a 46-GHz-f_T silicon bipolar process. The down-converter exhibits a SSB noise figure as low as 3.2 dB, a 24-dB power gain, and an input compression point of –23 dBm. It was assembled in a 4×4 mm^2 low-cost QFN 16-lead plastic package and draws only 18 mA from a 3-V power supply.**

I. Introduction

The success of cellular communications due to growing demands for mobility and flexibility has led to the remarkable development from wired to wireless LANs (WLANs). Indeed, in the 5-GHz license-exempt band there are two competing WLAN standards: ETSI HIPERLAN/2 and IEEE 802.11a. However, very few commercial products are available. At the moment, the lack of low-cost monolithic transceivers at 5-GHz represents an obstacle to the spread of mass-market equipment. The development of RF building blocks for this new generation of WLAN equipment must be based on VLSI silicon technologies, which should completely substitute expensive processes in the C-band.

With regards to RF down-conversion, both WLAN standards have very demanding dynamic range requirements, because the signal received can be very strong or very weak depending on transmitter-receiver distance and fading effects. This means that both low noise and high linearity have to be guaranteed. Moreover, power consumption must be reduced to the minimum to extent mobile equipment operating time.

Various silicon 5-GHz down-converters have been reported in literature and the most significant works are listed in Table I for comparison. All of these referenced down-converters have a SSB noise figure higher than 5 dB and a power gain lower than 20 dB with a similar linearity performance.

This paper presents the design and the on-board measurements of a 5-GHz down-converter, which was fabricated in a low-cost silicon bipolar technology. It achieves excellent gain and noise figure performance and good linearity is obtained with very low current consumption. Experimental results prove that pure silicon bipolar technology is very competitive in the C-band and can profitably be used for low-cost WLAN applications.

TABLE I
STATE OF THE ART OF 5-GHZ DOWN-CONVERTERS

Process	NF (dB)	Gain (dB)	Input IP_3 (dBm)	Current (mA)	Ref.
0.24 µm CMOS	5.2	12	-2	6.2	[1]
0.25 µm CMOS	6.4	—	-15	11.6	[2]
0.25 µm CMOS	3 (*DSB*)	18	-11	38	[3]
0.4 µm BiCMOS *22 GHz-f_T*	7 (*DSB*)	18	-17	18.5	[4]
0.5 µm SiGe BiCMOS *45 GHz-f_T*	7.5 (*DSB*)	12	-11	37	[5]
SiGe Bipolar *47 GHz-f_T*	5.9	19	-12	25	[6]
0.5 µm SiGe bipolar *47 GHz-f_T*	6.9	14	-5.8	27	[7]
Si Bipolar *25 GHz-f_T*	5.1	17	-4.5	23	[8]
Si Bipolar *46 GHz-f_T*	**3.2**	**24**	**-13**	**18**	**This work**

II. Circuit Description

A. Down-converter architecture

Fig. 1 shows the block diagram of the down-converter.

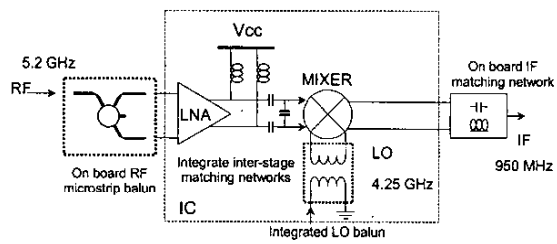

Fig. 1. Block diagram of the down-converter.

0-7803-7694-3/03/$17.00 © 2003 IEEE

The IC contains a low noise amplifier and a mixer, which down-converts the RF signal at 5.2 GHz to the IF at 950 MHz. The LO signal drives the mixer through an integrated staked balun. The overall circuit has a fully differential structure for better rejection of common mode spurious signals. To improve power gain and noise figure performance an inter-stage matching network is included, which uses integrated spiral inductors and high-Q metal-insulator metal (MIM) capacitors. It also provides a partial image rejection. An on-board microstrip rat-race is used to perform single to differential conversion. Output matching and differential to single conversion are achieved by means of an on-board discrete network.

B. Building-block schematics

Fig. 2 shows the simplified schematic of the low noise amplifier. A differential cascode structure with a resonant load is used. The cascode topology guarantees high input/output isolation. The resonant load provides both high gain and linearity. Indeed, inductors avoid DC voltage drop at the collectors. Optimum transistor sizing, inductive emitter degeneration and input bonding wires inductors allows simultaneous noise/input impedance matching [9].

The simplified schematic of the mixer is shown in Fig. 3. It uses a voltage to current (V-I) converter and a Gilbert quad. Degeneration inductors are used to increase linearity in the V-I converter. As mentioned above, the integrated LO transformer T drives the Gilbert quad performing single to differential conversion.

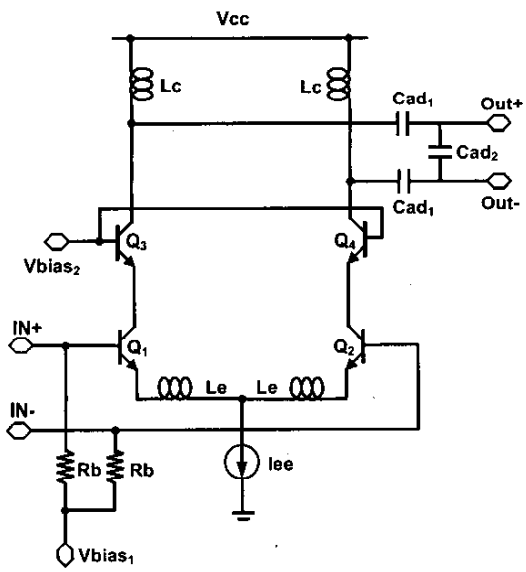

Fig. 2. Simplified schematic of the LNA.

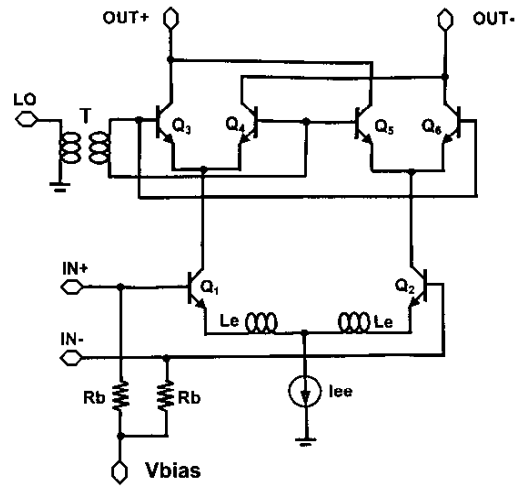

Fig. 3. Simplified schematic of the mixer.

III. Fabrication and Layout

The receiver was designed and fabricated in a 46-GHz-f_T double-poly self-aligned-emitter silicon bipolar process by STMicroelectronics (HSB3). It is a low-cost technology, requiring only 17 mask steps. It provides oxide trench isolation, three metal layers, poly resistors, pn-junction varactors and metal-insulator-metal (MIM) capacitors with 0.7 fF/μm^2. Spiral inductors and stacked transformers are built using the third and the second metal layers. In addition, an optional gold top metal layer is also available for higher quality factor inductors.

Fig. 4 depicts the die photograph of the down-converter.

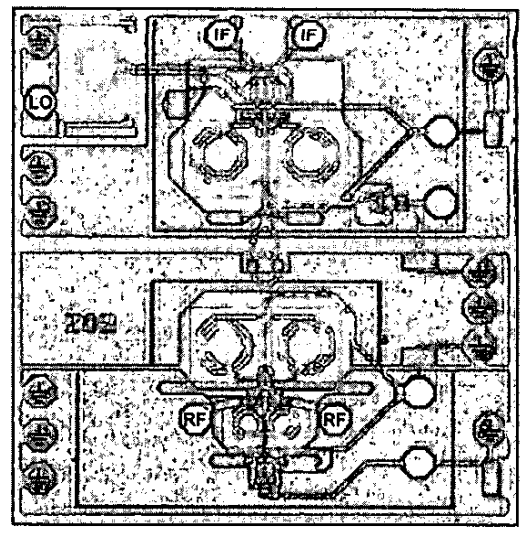

Fig. 4. Die photograph of the down-converter.

The overall die size is 1.8×1.8 mm^2 including bond pads. However, such a dimension mainly depends on package requirements, rather than on design needs. The layout has a vertical axis of symmetry. The LNA is placed at bottom and the mixer on the top. The RF and IF terminals are placed orthogonally to the LO input to reduce electromagnetic coupling through the bonding wires. The isolation between the LNA and the mixer is increased by using an oxide trench, guard-rings of substrate contacts surrounding each block and shielding metal ground planes. A separate ground terminal for the LO balun is also used.

III. Measurement Results

The chip was assembled in a 4×4 mm^2 low-cost QFN 16-lead plastic package and mounted on the evaluation board shown in Fig. 5.

At RF input, single to differential conversion was accomplished by a microstrip rat-race, whose loss is 0.8 dB. A 4:1 impedance ratio balun was used for the IF output network.

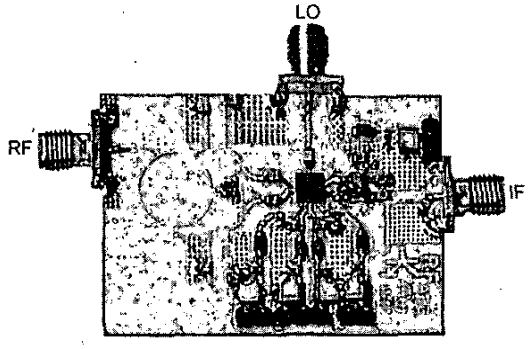

Fig. 5. Evaluation board.

Testing was carried out with a 3-V supply voltage and nominal bias currents. The mixer was driven by a –3 dBm LO signal. Raw measurements were corrected for the rat-race loss.

The power gain and the noise figure are shown in Fig. 6. The down-converter achieves a noise figure and a power gain of 3.2 dB and 24 dB, respectively. This performance agrees with what was expected, but it was measured at around 4.7 GHz instead of 5.2 GHz. In fact, the actual operating frequency differs by only 10 % from the simulated one. This discrepancy is due to a layout mistake on a capacitor in the inter-stage matching network. Of course, the performance at 5.2 GHz cannot be seen in Fig. 6 since inter-stage matching frequency greatly determines both power gain and noise figure.

The output spectrum for a –40 dBm RF signal at 4.7 GHz is depicted in Fig. 7.

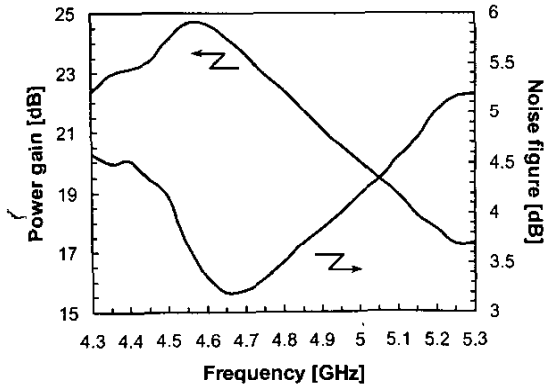

Fig. 6. Power gain and noise figure vs. frequency.

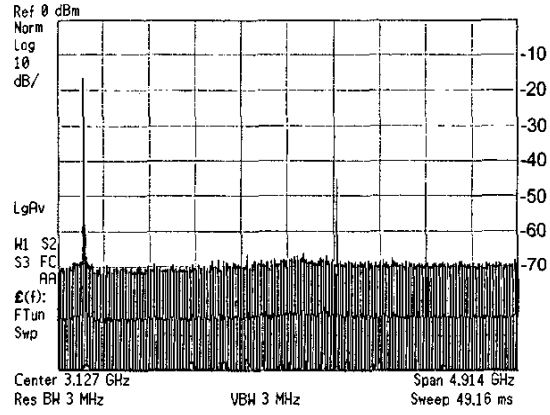

Fig. 7. Output spectrum.

The 950-MHz signal power is –16 dBm, the output spurious at LO and RF frequencies are –28 dBc and -30 dBc, respectively. A –23 dBm input-referred compression point was measured, as is shown in Fig. 8.

In Fig. 9 the power gain and the noise figure are given as a function of the LO signal power. They are almost independent of the LO over a wide range of power levels.

An LO-RF isolation of 60 dB was measured. Finally, the input and output return losses were –10 dB and –12 dB, respectively. The down-converter draws only 18 mA from a 3-V power supply.

The measurements are summarized in Table II.

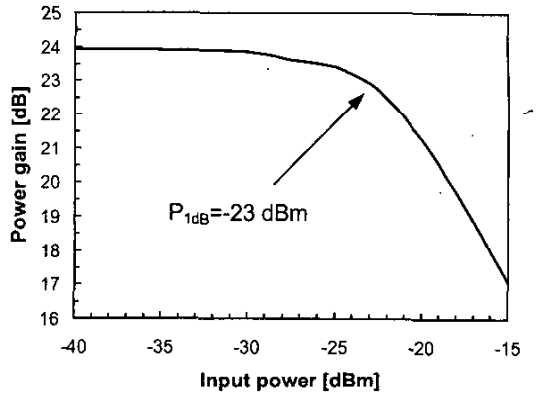

Fig. 8 Power gain vs. input power.

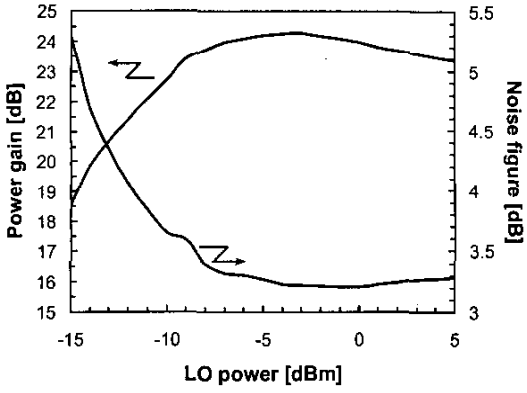

Fig. 9. Power gain and noise figure vs. LO signal power.

TABLE II
DOWN-CONVERTER MEASUREMENTS

Operating Frequency	4.7 GHz
LO Frequency	3.75 GHz
IF Frequency	950 MHz
Power Gain	24 dB
1-dB Input Compression Point	-23 dBm
Input IP3	-13 dBm
Noise Figure	3.2 dB
Image Rejection	35 dB
LO-IF Isolation	42 dB
LO-RF Isolation	60 dB
S11	-10 dB
S22	-12 dB
Current Dissipation	18 mA
Supply Voltage	3 V
Area	3.2 mm^2

V. CONCLUSION

A 5-GHz monolithic down-converter built in a low-cost pure bipolar technology has been presented. It provides a SSB noise figure as low as 3.2 dB, a power gain as high as 24 dB, and an input compression point of –23 dBm. This excellent performance was achieved with a current consumption of only 18 mA from a 3-V power supply.

ACKNOWLEDGEMENT

This work was supported by the IST "PERLA" project of EU. The authors would like to thank A. Castorina of STMicroelectronics for his precious assistance in carrying out measurements.

REFERENCES

[1] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS Wireless LAN Receiver Front End," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765-771, May 2000.

[2] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection," *IEEE J. of Solid-State Circuits*, vol. 36, no. 5, pp. 810-814, May 2001.

[3] T. P. Liu, and E. Westerwick, "5-GHz CMOS Radio Tranceiver Front-End Chipset," *IEEE J. Solid-State Circuits*, Vol. 35, no. 12, pp. 1927-1933, Dec. 2000.

[4] M. Madihian, T. Drenski, L. Desclos, H. Yoshida, H. Hirabayashi, and T. Yamazaki, "A 5-GHz-Band Multifunctional BiCMOS Transceiver Chip for GMSK Modulation Wireless Systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 25-31 Jan. 1999.

[5] J. O. Plouchart, H. Ainspan, M. Soyuer, "A 5.2 GHz 3.3 V I/Q SiGe RF Transceiver," *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 217-218.

[6] M. A. Copeland, S. P. Voinigescu, D. Marchesan, P. Popescu, and M. C. Malerpard, "5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering," *IEEE Trans. Microwave Theory and Tech.*, vol. 48, no. 2, pp. 170-180, Feb. 2000.

[7] J. R. Long, "A Low-Voltage 5.1-5.8 GHz Image-Reject Downconverter RF IC," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1320-1328, Sept. 2000.

[8] J. P. Maligeorgos and J. R. Long "A Low-Voltage 5.1-5.8-GHz Image-Reject Receiver with Wide Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1917-1925, Dec. 2000.

[9] G. Girlando, and G. Palmisano "Noise Figure and Impedance Matching in RF Cascode Amplifiers". *IEEE Trans. Circuit Syst. II*, vol. 46, no. 11, pp. 1388-1396, Nov. 1999.